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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/068,768	02/06/2002	Matthew S. Von Thun	02-0003 1496.00201	9287

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EXAMINER	
LE, DINH THANH	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 01/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/068,768	THUN ET AL.	
	Examiner	Art Unit	
	DINH T. LE	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 November 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-5,7-11 and 13-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *20* is/are allowed.

6)☒ Claim(s) *1,3-5,7-11,13-18 and 26* is/are rejected.

7)☒ Claim(s) *19 and 21-25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

FINAL REJECTION

Response to Applicant's Amendment

Claim Rejections

Claim Rejections - 35 USC § 112

Claims 1, 3-5, 7-11, 13-17 and 21-26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction or clarification is required.

In claim 1, the recitation "a voltage drop from said first gate to said . . . input voltage" on lines 13-15 is unclear and as such indefinite. It is not understood what the function of the input voltage is, how the voltage can be "non-linear" and how this limitation is read on the preferred embodiment. Insofar as understood, no such limitation is seen on the drawings. The same is true for claims 11.

In claim 26, it is unclear how the second stage can be "configured " to cancel the voltage level shift at the first output.

The remaining claims are depending upon the above rejected claims and therefore also considered indefinite.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-5, 10, 11, 13 and 14, are rejected under 35 USC 103 (a) as being unpatentable over Lien (US 6,441,651) in view of Talaga, Jr. (US 5,942,921)..

Lien discloses in Figure 7 a source follower circuit (700) comprising a NMOS transistor (501) having a first gate (G) configured to receive an input voltage (Vin), a first drain (D) coupled to a first supply voltage (VCC), a first resistive element (701) having a first side coupled to a first source (S) of the NMOS transistor (501) and a second side configured to receive a second voltage (VSS). However, Lien does not disclose that the input voltage ranges from up to twice the first supply with respect to at the second supply voltage. Talaga, Jr. teaches a source follower in Figure 3 comprising the transistor (306) coupled to a resistor (308) and the transistor (306) is designed to range up to at least twice the power supply voltage without causing the transistor failure so that the transistor can handle the input voltage which exceeds the supply voltage without requirement that a higher power supply voltage will be provided, see column 2, lines 1-6 and column 3, lines 25-33. It would have been obvious to a person having skill in the art at the time the invention was made to modify the transistor of Lien to handle the input voltage up twice the supply voltage taught by Talaga, Jr. for the purpose of handling the higher input voltage without the requirement that a higher power supply voltage will be provided.

Note that the maximum voltage drop across the gate oxide of the modified transistor of Lien would not exceed a difference between the supply voltage (VCC) and the second supply voltage (ground). For example, suppose that the VCC is equal to 3V, then the maximum input voltage VIN would be equal to 6V. Therefore, the maximum gate oxide voltage would be equal to 6V-3V= 3V. Also, selecting the NMOS transistor or the native NMOS device would be

obvious and considered to be a matter of design expedient for an engineer since both the transistor perform an equivalent function of a switch.

Also, as well known in the art, the change of the gate-source voltage, i.e., the transistor (501) of Lien, inherently would not increase linearly to the change of the gate voltage after the transistor (501) is in the saturation state. Thus, the voltage drop from the gate to the output of the transistor is "non-linear" as a function of the input voltage."

Claims 1, 3-5, 7-11 and 13-17 are rejected under 35 USC 103 (a) as being unpatentable over Ito et al (US 5,218,247) in view of Lien US 6,441,651) and furthering view of Talaga, Jr. (US 5,942,921).

Ito et al discloses in Figure 3 a source follower circuit comprising a PMOS transistor (13) coupled to a first resistor (15) and a NMOS transistor (14) coupled to a second resistor (14). Wherein the sources of the transistors (13, 14) are coupled to the output terminal (34). However, Ito et al does not disclose that the transistors are the gate oxide and the input voltage ranges up to twice the supply voltage (VDD). Lien teaches in Figure 7 a source follower circuit comprising a gate oxide transistor (501) for minimizing the voltage across the gate oxide, column 1, lines 35-37 but does not disclose that the input voltage ranges up to twice the supply voltage. Talaga, Jr. (Talaga) teaches a source follower circuit in Figure 3 comprising a transistor (406) and resistor (408), and the transistor (406) is configured to have the input voltage VIN ranges up to at least twice the power supply voltage (VCC) , column 3, lines 25-33, so that the transistor can handle the input voltage higher than the supply voltage without replacing the higher supply voltage. It would have been obvious to a person having skill in the art at the time

the invention was made to employ the transistors taught by Line and Talaga in the circuit of Ito et al for the purpose of minimizing the gate oxide voltage and handling the input voltage higher than the power supply voltage without replacing the supply voltage with a higher supply voltage.

Claim 18 is rejected under 35 USC 103 (a) as being unpatentable over Goto et al (US 4,760,287) in view of Lien (US 6,441,651) and further in view of Talaga , Jr. (US 5,942,921).

Goto et al discloses in Figure 12 a cascaded source follower circuit comprising a first transistor (34) coupled to a first current source (resistor 53) and a second transistor (44) coupled to a second current source (resistor 54) but does not disclose that the transistors are the gate oxide and the input voltage ranges up twice the supply voltage (VDD). Lien teaches in Figure 7 a source follower circuit comprising a gate oxide transistor (501) for minimizing the voltage across the gate oxide, column 1, lines 35-37, but does not disclose that the input voltage ranges up to twice the supply voltage. Talaga, Jr. (Talaga) teaches a source follower circuit in Figure 3 a source follower circuit comprising a transistor (406) and resistor (408); wherein the transistor (406) is configured to have the input voltage VIN ranges up to at least twice the power supply voltage (VCC) , column 3, lines 25-33, so that the transistor can handle the input voltage higher than the supply voltage without replacing the supply voltage with a higher supply voltage. It would have been obvious to a person having skill in the art at the time the invention was made to employ the transistors taught by Lien and Talaga in the circuit of Ito et al for the purpose of minimizing the gate oxide voltage and handling the input voltage higher than the power supply without replacing the supply voltage with a higher supply voltage.

Response to Applicant's Arguments

The applicant argues that Lien, Ito and Talaga are silent regarding a non-linear transfer characteristic. The argument is not persuasive because after saturation, the gate source voltage, i.e., the transistor (501) of Lien, does not change linearly to the change of the gate voltage. Thus, the voltage drop from the gate to the output of the transistor is "non-linear as a function of the input voltage."

The applicant argues that neither the current source 53 nor the current source 54 in FIG. 12 of Goto is a resistor. Therefore, the Office Action has failed to establish prima facie obviousness for lack of a first resistive element and a second resistive element as presently claimed. The argument is not persuasive because, as well known in the art, the resistor is a current source.

The applicant argues that of Ito shows the source node 53 of transistor 13 directly connected to a gate of a transistor 21 and a source node 54 of transistor 14 directly connected to a gate of a transistor 22. Ito appears to be silent regarding the source nodes S3 and 54 being directly connected to a common output. Therefore, Ito, Lien and Talaga, alone or in combination, do not appear to teach or suggest a first source of a first device and a second source of a second device directly coupled to an output as presently claimed. contrast,

Allowable Subject Matter

Claim 20 is allowed.

Claims 19 and 21-25 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

The claims would be allowable over prior art of record because the prior art does not disclose the multiplexer and the first source of the first device and the second source of the second device being connected "directly" to the output.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Dinh Le whose telephone number is (703) 305-3790. The examiner can normally be reached on Monday to Friday from 7:00 A.M.to 5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 308-4876. The fax phone number for this Group is (703) 308-7725.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

DINH LE
Primary Examiner

January 21, 2004